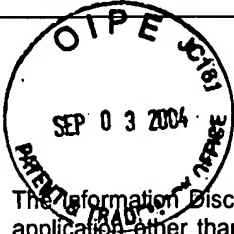


TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT Under 37 CFR 1.97(b), (c), or (d)			Docket No. YOR920030469US1
In re Application of: Cabral, et al.			
Serial No. 10/669,898	Filing Date September 24, 2003	Examiner	Group Art Unit
Title: METHOD AND APPARATUS FOR FABRICATING CMOS FILED EFFECT TRANSISTORS			



Address to:
 Commissioner for Patents
 Alexandria, VA 22313-1450

37 CFR 1.97(b)

1. ☒ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits; or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

37 CFR 1.97(c)

2. ☐ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), but prior to the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by the statement or fee as indicated below.

37 CFR 1.97(d)

3. ☐ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(c), but on or before payment of the issue fee and is accompanied by the statement and fee as indicated below.

Required Statements and/or Fees Under 37 CFR 1.97(c) or (d)

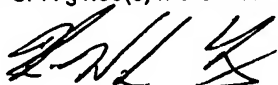
☐ Each item of information contained in the accompanying Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Information Disclosure Statement. (37 CFR 1.97(e)(1))

☐ No item of information in the accompanying Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned person, after making reasonable inquiry, no item of information contained in the accompanying Information Disclosure Statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the Information Disclosure Statement. (37 CFR 1.97(e)(2))

☐ The fee set forth in 37 CFR 1.17(p). Please credit any overpayment or charge any insufficiencies to deposit account number 20-0782.

37 CFR §1.704(d)

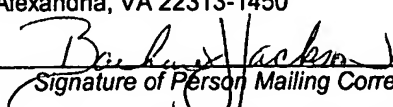
4. ☐ Each item of information in the accompanying Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in 37 CFR §1.56(c) more than thirty days prior to the filing of the Information Disclosure Statement.


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Dated: 8/31/04

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Barbara J. Jackson
 Typed or Printed Name of Person Mailing Correspondence

U.S. Department of Commerce, Patent and Trademark Office (PTO Form 1449 modified)		Docket No. YOR920030469US1	Serial No. 10/669,898
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicant Cabral, et al.	Confirmation No.:
(Use several sheets if necessary)		Filing Date 09/24/2003	Group
Examiner			

U.S. Patent Documents

*Examiner Initial		Document Number	Issue Date	Applicant(s) Name	Class	Subclass	Filing Date If Appropriate
	A1						
	A2						
	A3						
	A4						
	A5						
	A6						
	A7						
	A8						

Foreign Patent Documents

*Examiner Initial		Document Number	Date	Country	Class	Subclass	Translation	
							YES	NO
	B1						<input type="checkbox"/>	<input type="checkbox"/>
	B2						<input type="checkbox"/>	<input type="checkbox"/>
	B3						<input type="checkbox"/>	<input type="checkbox"/>
	B4						<input type="checkbox"/>	<input type="checkbox"/>

OTHER ART

*Examiner Initial		Including Author, Title, Date, Pertinent Pages, Etc.
	C1	Kedzierski, et al., "Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation," International Electron Devices Meeting, Conference Digest, December 2002, Page(s): 247 -250
	C2	Krivokapic, et al., "Nickel Silicide Metal Gate FDSOI Devices with Improved Gate Oxide Leakage," IEDM 2002, pp. 271-274.
	C3	Maszara, et al., "Transistors with Dual Work Function Metal Gates by Single Full Silicidation (FUSI) of Polysilicon Gates," AMD 2002 Analyst Meeting, November 7, 2002
	C4	Qin, et al., "Investigation of Polycrystalline Nickel Silicide Films as a Gate Material," J. the Electrochemical Soc., 148(5), G271-G274, (2001)

Examiner	Date Considered
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.	